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(54) Semiconductor integrated circuit.

(57) In a semiconductor integrated circuit having a plurality writable/readable memory blocks (M4, M5) with different address spaces and an address decoder for selecting address of the memory blocks (M4, M5), multiple memory blocks (M4, M5) are permitted to share part of addresses in test mode of the memory blocks (M4, M5), and writing in a memory block (M4) other than the memory block (M5) having the largest address space is disabled during a period in which address signals for commonly performing address scan of individual memory blocks (M4, M5) exceeds the address width of that memory block (M4). It is therefore possible to permit a plurality of memory blocks (M4, M5) with different address spaces mounted on the same chip to be tested at a time with a high precision and without putting any burden on the generation of test vectors or a test circuit for a BIST method.

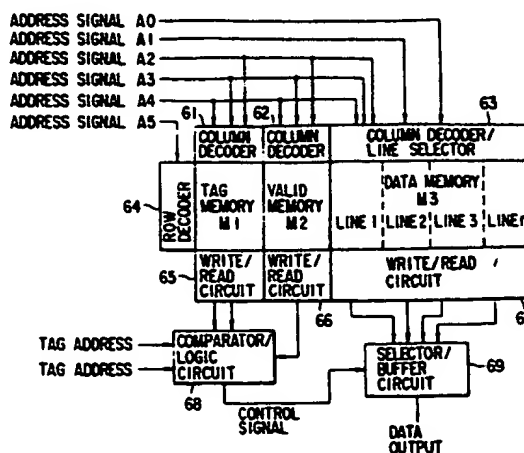


FIG. 1

The present invention relates to a semiconductor integrated circuit and, more particularly, to a test circuit that facilitates testing of an integrated circuit mixedly including a large capacity memory circuit and a logic circuit, for example.

Conventionally, in hybrid integrated circuits having multiple memory blocks mounted on the same chip, a structure (e.g., a cache memory) where share the addresses of the individual memory blocks or a structure where a test circuit or the like shares the addresses of the individual memory blocks is often used. In this case, as described hereinafter, it is difficult to improve the precision of detecting defects originating from a memory blocks and increase the testing efficiency, e.g., shortening the testing time, when a test is conducted to check the functions of a memory circuit.

The methods of testing memory circuits having the above structure are classified into two general categories. One is to use a tester or the like to supply the necessary signals to the memory circuit from outside the integrated circuit, and the other is a BIST (Built-In Self Testing) method which allows the device itself to produce the required test signals to conduct the test. In conducting such tests, the test efficiency will be improved if multiple memories are tested at a time using the shared addresses. However, the address spaces of different memory blocks should not often necessarily be the same.

Fig. 1 is a block diagram exemplifying an arrangement of a cache memory. A tag memory M1, a valid bit memory M2 and a data memory M3 having multiple lines have different address spaces. A column decoder 61 selects column address of the tag memory M1 using address signals A2 to A4. A column decoder 62 selects column address of the valid bit memory M2 using the address signals A2 to A4. A column decoder/line selector 63 selects a column address and a line for the data memory M3 using address signals A0 to A4. A row decoder 64 commonly selects row address of the individual memory blocks M1, M2 and M3 based on an address signal A5. A reference numeral 65 denotes a write/read circuit for the tag memory M1; 66, a write/read circuit for the valid bit memory M2; and 67 a write/read circuit for the data memory M3. A comparator/logic circuit 68 compares an tag address input with tag data which is read from the tag memory M1, checks valid bit data consisting of bits 1 to 4 and read from the valid bit memory M2, and outputs a control signal. A selector/buffer circuit 69 selectively outputs data which are read from multiple lines of the data memory M3, based on the control signal from the comparator/logic circuit 68.

The individual memory blocks M1, M2 and M3 share the address signals A2 to A5 of the address

signals A0 to A5. However, the memory blocks M1 and M2 have narrower address space than the memory block M3 by the address signals A1 and A0. Therefore, when a test is conducted on the above cache memory based on the address of the data memory M3 having large address space, the tag memory M1 and the valid bit memory M2 will access the same address multiple times while the entire addresses of the data memory M3 are circulated once. This will not be significant so much in a simple memory test, but will matter when a memory test is performed with an improved high precision.

Figs. 2A through 2C show examples of vectors of an N-system pattern (March) typically used in memory tests. A reference numeral 71 shows the size of a memory block, and 72 indicates the direction where the addresses are advanced. First, a value "0" is written in the entire memory cells from a smaller address to a larger one in Fig. 2A, then the value "0" is read from each memory cell, and then the value "1" is written in the same memory cell in Fig. 2B. In Fig. 2C, the value "1" is read from the memory cells from a larger address to a smaller one and the value "0" is then written in the same memory cell, as indicated by the vector directing opposite to the one in Fig. 2A.

Figs. 3A and 3B are diagrams for explaining the relationship between the address signals of a memory block and cell block selection when the cache memory in Fig. 1 is tested in accordance with the memory test vectors as shown in Fig. 2. Fig. 3A illustrates the relationship between the address signals of the tag memory M1 and valid bit memory M2, which have small address space, and the cell block selection. Fig. 3B illustrates the relationship between the address signals of the data memory M3 having large address space, and the cell block selection. As shown in Fig. 3A-I, in the memory blocks M1 and M2 having small address space, the memory cell ① is accessed when the address signals A2 and A3 are (0, 0). It is apparent from Fig. 3A-II that multiple accesses to the memory cell ① are caused during when the address signals A2 and A3 are scanned sequentially from (0, 0) to (0, 1), (1, 0) and (1, 1) since the address signals A2 and A3 stay (0, 0) during such address scanning. On the other hand, each memory cell in the data memory M3 is accessed by the address signals A0, A1, A2 and A3, as shown in Fig. 3B-I. In accordance with scanning of the address signals A0, A1, A2 and A3, therefore, the individual memory cells ①, ②, ③ and ④ are accessed sequentially, as shown in Fig. 3B-II. In other words, a memory having small address space will access the same memory cells multiple times while an address not associated with the memory itself, i.e., an address of a memory having large address

space is being accessed. In this situation, since multiple writings will be caused in a single sequence on the same cell of the memory with small memory space, the read output is likely to differ from the expected value.

With the use of a tester, this situation can be cleared by properly designing the test vectors. However, since test vectors for solid writing are normally used, this measure requires a huge number of vectors in proportion to the address space of a memory to be tested and is not thus practical. For instance, if the tested memory is an 8K-byte memory, an N^2 -system pattern for the memory needs 65 M bytes. It is therefore typical to employ a method of automatically generating an address by a tester. However, it is difficult to avoid the multiple accesses with this measure.

According to the BIST method, the memory itself automatically generates address signals and write data and compares data to test memory blocks. However, when it is necessary to test a memory with a more complex address pattern due to an increased capacity of memory blocks, the difference between the address spaces of multiple memory blocks would be critical. It would result in an increased testing time and an increased overhead of hardware, i.e., testing circuit.

Since a memory test for conventional semiconductor integrated circuits should be conducted for each of multiple memory blocks with different address spaces mounted on the same chip, a longer testing time is required, otherwise, a large burden will be put on the test circuit or the generation of test vectors.

It is therefore an object of the present invention to provide a semiconductor integrated circuit which permits multiple memory blocks with different address spaces mounted on the same chip to be tested at a time with a high precision and without putting any burden on the generation of test vectors or the test circuit for use in a BIST method.

According to an aspect of the present invention, there is provided a semiconductor integrated circuit comprising: a plurality of writable/readable memory blocks with different address spaces mounted on a same chip; means for performing address scanning on the writable/readable memory blocks simultaneously in test mode based on one memory block which has a largest address space the memory blocks; and control means for disabling writing in other memory blocks having a smaller address space than the largest address space during an address scan period exceeding address widths of the other memory blocks.

According to another aspect of the present invention, there is provided a semiconductor integrated circuit comprising: a writable/readable first memory block having a first address space; at least

one writable/readable second memory block, mounted on a same chip as the first memory block and having an address space smaller than the first address space, the second memory block and the first memory block sharing part of an addresses in normal operation mode; means for supplying address signals to simultaneously and commonly scan addresses of the first and second memory blocks in test mode; an address decoder for selecting addresses of the first and second memory blocks based on the address scan signal; and a control circuit for disabling write/read operations on the second memory block in the test mode during a period in which the address signals exceed the address space of the second memory block.

According to still another aspect of the present invention, there is provided a semiconductor integrated circuit comprising: a writable/readable first memory block having a first address space; at least one writable/readable second memory block, mounted on a same chip as the first memory block and having an address space smaller than the first address space, the second memory block and the first memory block not sharing part of addresses in normal operation mode; a logic circuit, mounted on the same chip as the first memory block, for supplying address signals to simultaneously and commonly scan addresses of the first and second memory blocks in test mode; an address selector for selecting part of address signals to perform address scan of the first memory block and generating address signals of the second memory block in test mode; an address decoder for selecting addresses of the first and second memory blocks based on the address signals from the logic circuit and the address selector; and a control circuit for disabling write/read operations on the second memory block in the test mode during a period in which the address signals of the first memory block exceeds the address space of the second memory block.

According to still another aspect of the present invention, there is provided a semiconductor integrated circuit comprising: a writable/readable first memory block having a first address space; at least one writable/readable second memory block, mounted on a same chip as the first memory block and having an address space smaller than the first address space, the second memory block and the first memory block not sharing part of addresses in normal operation mode; a self-testing address generator, mounted on the same chip as the first memory block, for supplying address signals to simultaneously and commonly scan addresses of the first and second memory blocks in test mode; an address selector for selecting the address signals to generate address signals of

each of the memory blocks in test mode; an address decoder for selecting addresses of the first and second memory blocks based on the address signals from the address selector; and a control circuit for disabling write/read operations on the second memory block in the test mode during a period in which the address signals to commonly perform address scan of the memory blocks exceeds the address space of the second memory block.

In normal operation mode of the individual memory blocks, the addresses are selected based on address signal inputs associated with each memory block, and write/read operations are then performed. In test mode of the individual memory blocks, the addresses of the first memory block are scanned by address signals having an address width corresponding to the largest address space among multiple memory blocks, and write/read operations of the memory block are performed. At the same time the addresses of a memory block having a smaller address space are scanned by part of the address signals, and write/read operations for the memory block are carried out. In this case, writing operations of the memory block having a smaller address space are disabled for a while in which the address width of the address signals exceeds the address width of this memory block, i.e., while an address space irrelevant to this memory block is being designated.

With the above, it is possible to eliminate the unnecessary memory access to a memory block having a small address space, and it is also possible to simultaneously test multiple memory blocks with different address spaces and mounted on the same chip with a high precision, without putting any burden on the generation of test vectors or the test circuit for a BIST method.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an arrangement of a conventional cache memory;

Figs. 2A through 2C are diagrams for explaining memory test vectors;

Figs. 3A-I and 3A-II are diagrams for explaining the relationship between the address signals of a memory block and cell block selection when a memory block having a small address space in Fig. 1 is tested in accordance with the memory test vectors as shown in Figs. 2A to 2C;

Figs. 3B-I and 3B-II are diagrams for explaining the relationship between the address signals of a memory block and cell block selection when a memory block having a large address space in Fig. 1 is likewise tested;

Fig. 4 is a block diagram illustrating an arrange-

ment of the first embodiment of a semiconductor integrated circuit according to the present invention;

Figs. 5A-I and 5A-II are diagrams for explaining the relationship between the address signals of a memory block and cell block selection when a memory block having a small address space in Fig. 4 is tested;

Figs. 5B-I and 5B-II are diagrams for explaining the relationship between the address signals of a memory block and cell block selection when a memory block having a large address space in Fig. 4 is likewise tested;

Fig. 6 is a block diagram illustrating an arrangement of the second embodiment of a semiconductor integrated circuit according to the present invention;

Fig. 7 is a block diagram illustrating an arrangement of the third embodiment of a semiconductor integrated circuit according to the present invention; and

Fig. 8 is a block diagram illustrating an arrangement of the fourth embodiment of a semiconductor integrated circuit according to the present invention.

Semiconductor integrated circuits according to preferred embodiments of the present invention will now be described referring to the accompanying drawings.

Fig. 4 is a block diagram illustrating an arrangement of the first embodiment of a semiconductor integrated circuit according to the present invention. Fig. 4 shows a hybrid integrated circuit in which multiple (two in this embodiment) writable/readable memory blocks M4 and M5 with different address spaces and a logic circuit (not shown) such as a CPU (Central Processing Unit) are mounted on the same chip. Two memory blocks M4 and M5 are a tag/valid bit memory M4 and a data memory M5 in a cache memory, for example. As means for selecting the addresses of the memory blocks M4 and M5, a column decoder 11, a column decoder/line selector 12 and a row decoder 13 are provided. The column decoder 11 selects the column addresses of the memory block M4 using address signals A2 to A4. The column decoder/line selector 12 selects the column addresses of the memory block M5 using address signals A0 to A4. The row decoder 13 commonly selects row addresses for both memory blocks M4 and M5 using address signals A5 and A6. More particularly, two memory blocks M4 and M5 share the address signals A2 to A6 of the address signals A0 to A6, and the memory block M4 has a smaller address space by the address signals A1 and A0 than the memory block M5. Further, a write/read circuit 14 for performing write/read operations on the memory block M4 and a write/read circuit 15

for performing write/read operations on the memory block M5 are provided. A write/read control signal W/R is directly input to the write/read circuit 15. A write/read control signal W/R from a control circuit 16 is input to the write/read circuit 14. The control circuit 16 receives the address signals A1 and A0, part of the address signals A0 to A6, the write/read control signal W/R and a mode designation signal MODE. The control circuit 16 is constituted of a logic circuit. The control circuit 16 outputs the received write/read control signal as it is in normal operation mode, but, in test mode, it decodes the address signals A1 and A0 and outputs the received read/write control signal as it is or a write disable control signal W-INH in accordance with the results of the decoding an inverted signal of the write control signal, for example, the read control signal in this embodiment. More specifically, in test mode, the control circuit 16 outputs the write/read control signal W/R as it is only when the combination of the address signals A1 and A0, part of the address signals A0 to A6, matches with a predetermined pattern, e.g., only when both the address signals A1 and A0 are "0," though such is arbitrarily determined in accordance with the memory structure. However, when the combination of the address signals A1 and A0 is other than the predetermined pattern, e.g., when either one of the address signals A1 and A0 is "1" in test mode the circuit 16 does not output the received write/read control signal W/R as it is, but the write disable control signal W-INH. This corresponds to the case where the address signals have an address width exceeding the address width of the memory block M4 or they designate address space not associated with the memory block M4.

The operation of the integrated circuit in Fig. 4 in test mode will now be discussed referring to Figs. 5A and 5B. First, in normal operation mode of each memory block, addresses are selected on the basis of the address signals A0 to A3 corresponding to each memory block M4 or M5, and the associated write/read operations are performed. Then, in test mode of each memory block, cell blocks of each memory block M4 or M5 are selected, as shown in Figs. 5A and 5B. More specifically, when the address signals A0 to A6 having an address width corresponding to that of the memory block M5 which has the largest address space are input, the addresses of the memory block M5 are scanned as shown in Fig. 5B-I. Memory cells ①, ②, ③, ④, ⑤, ... are sequentially accessed for their write/read operations, as shown in Fig. 5B-II. At the same time, the addresses of the memory block M4 are scanned by the address signals A2 to A6 of the address signals A0 to A6 as shown in Fig. 5A-I, followed by write/read operations as shown in Fig. 5A-II. During a period in which the

length of the address signals A0 to A6 exceeds the address width of the memory block M4 (in which address space not associated with the memory block M4 is being specified), i.e., when at least either one of the address signals A1 and A0 is "1," write operations on the memory block M4 are automatically disabled by the write/read disable control signal W/R-INH, thus preventing multiple accessing. In test mode, data read from the memory blocks M4 and M5 are outputted to, for example, the outside of the integrated circuit.

At the time a memory test is to be conducted, therefore, the address space of the memory block M5 has only to be considered. This makes it possible to eliminate unnecessary memory accessing and to simultaneously test multiple memory blocks without putting any burden on the generation of test vectors.

As a modification of the first embodiment, the control circuit 16 in Fig. 4 may be omitted. The write/read control signals are inputted to the write/read circuit 14 of the memory block M4 in normal operation mode, while the write/read disable signals are inputted externally in test mode.

The present invention may also be applied in the case where more complicated memory accessing than done in the first embodiment is carried out.

Fig. 6 is a block diagram illustrating an arrangement of the second embodiment of a semiconductor integrated circuit according to the present invention. Fig. 6 shows a hybrid integrated circuit in which multiple (two in this embodiment) writable/readable memory blocks M4 and M5 with different address spaces and other blocks than the memory blocks, e.g., logic circuits 38 and 39, are mounted on the same chip. In the second embodiment, the present invention is applied to an integrated circuit which disables signals of the memory blocks inside in normal operation mode, and can directly access the memory blocks only in test mode. A memory block M6 has a smaller address space, and an address decoder 31 selects the addresses of the memory block M6. A memory block M7 has a larger address space, and an address decoder 32 selects the addresses of the memory block M7. A write/read circuit 34 controls write/read operations of the memory cells in the memory block M6. A write/read circuit 35 controls write/read operations of the memory cells in the memory block M7. A control circuit 36 receives a write/read control signal W/R, a mode designation signal MODE and address signals A0 and A1. According to the second embodiment, a logic circuit 38 outputs the address signals A0 to A3 and the write/read control signal W/R. The mode designation signal MODE is supplied externally. Data output from the memory blocks M6 and M7 are

supplied to a logic circuit 39. The control circuit 36 operates in the same manner as the control circuit 14 shown in Fig. 4.

In addition to the above-described effect of the first embodiment, the second embodiment can accomplish parallel tests of multiple memory blocks at a time without putting any burden on test vectors even when further miniaturization of an integrated circuit is pursued as the capacity of the memories mixedly mounted on the integrated circuit significantly increases, and thus the memories of the integrated circuit needs to be subjected to the same test as that for a general-purpose memory. This feature is very effective because it improves the testing efficiency, such as shortening the testing time.

Fig. 7 is a block diagram illustrating an arrangement of the third embodiment of a semiconductor integrated circuit according to the present invention. Fig. 7 shows the present invention as applied to a hybrid integrated circuit in which multiple (two in this embodiment) writable/readable memory blocks M8 and M9 with different address spaces and other blocks than the memory blocks, e.g., logic circuits 48 and 49, are mounted on the same chip, and in which multiple memory blocks do not share the same address in normal operation mode, i.e., their addresses are selected by different address signals. An address selector 40 is controlled in accordance with the mode designation signal MODE. The address selector 40 selects address signals A4 and A5 of the memory block M8 with a smaller address space in normal operation mode. In test mode, the address selector 40 selects address signals A2 and A3 among the addresses signals A0 to A5 with an address width corresponding to the memory block M9 having a larger address space. The selector 40 then converts the signals A2 and A3 into signals A4 and A5, which are, in turn, sent to an address recorder 41 of the memory block M8. The address signals A0 to A5 and the write/read control signal W/R are supplied from a logic circuit 48. The mode designation signal MODE is supplied externally. The operation of the control circuit 46 is essentially the same as that of the control circuit 36.

The third embodiment produces the same effect as the second embodiment by the memory blocks sharing part of the addresses temporarily, e.g., only in test mode.

Fig. 8 is a block diagram illustrating an arrangement of the fourth embodiment of a semiconductor integrated circuit according to the present invention. Fig. 8 shows the present invention as applied to a hybrid integrated circuit in which multiple (two in this embodiment) writable/readable memory blocks M10 and M11 with different address spaces and other blocks than the memory

blocks, e.g., logic circuits (not shown), are mounted on the same chip, and in which multiple memory blocks do not share the same address in normal operation mode. In the fourth embodiment, a BIST method is employed to facilitate the memory test. A BIST control circuit 59 receives a BIST control signal and write/read control signal W/R, and outputs an address generation control signal to a self-testing address generator 50. The address generator 50 generates test address signals TA0 to TA4 in test mode. An address selector 57 externally receives the address signals A0 to A2 and sends them to a decoder 51 in normal operation mode. However, the selector 57 selects the test address signals TA0 to TA2 of the test address signals TA0 to TA4 from the self-testing address generator 50 and sends them to the address decoder 31 in test mode. An address selector 58 externally receives the address signals A0 to A4 and sends them to a decoder 52 in normal operation mode, while it selects the test address signals TA0 to TA4 from the self-testing address generator 50 and sends them to the address decoder 32 in test mode. The BIST control circuit 59 outputs a test mode signal to the address selectors 57 and 58 and control circuit 56, and further outputs a write/read control signal W/R to the control circuit 56 and a write/read circuit 55 of the memory block M11. A BIST data generator/comparator 53 generates self-test data and sends then to a write/read circuit 54 and the write/read circuit 55. The comparator 53 then compares read outputs from the circuits 54 and 55 with an expected value previously prepared. The BIST control circuit 59 further exchanges the BIST data generation control signal and comparison outputs by the BIST data generator/comparator 53, and outputs the result of self-testing. The control circuit 56 receives the test address signals TA3 and TA4 from the self-testing address generator 50 in addition to the write/read control signal W/R and test mode signal TEST. In test mode, the circuit 56 sends an output to disable write/read operations on the memory block M10 with respect to the address signals TA3 and TA4 to the BIST data generator/comparator 53.

According to the fourth embodiment, the BIST method is employed to facilitate testing of memory blocks, and multiple memory blocks share part of the address in test mode. In the case where a memory test should be conducted with a more complicated address pattern due to an increased capacity of each memory block, therefore, it is possible to suppress the BIST-originated hardware restriction and overhead. Thus parallel testing of multiple memory blocks is ensured without burdening a testing circuit or the like and the testing efficiency such as shortening of the testing time is improved. The fourth embodiment is therefore very

effective.

As described above, the semiconductor integrated circuit embodying the present invention can permit multiple memory blocks with different address spaces mounted on the same chip to be tested at a time as well as ensure even a memory test involving complicated address accessing with a high precision and without putting any burden on the generation of test vectors or a testing circuit for a BIST method. This feature can significantly improve the testing efficiency, such as shortening of the testing time, as compared with the conventional case where a memory test is conducted with high precision only for each of memory blocks at a time at the price of an increased testing time, and is thus very effective.

Claims

1. A semiconductor integrated circuit comprising:
 - a plurality of writable/readable memory blocks (M4, M5; M6, M7; M8, M9; M10, M11) with different address spaces mounted on a same chip;
 - means for performing address scanning on said writable/readable memory blocks (M4, M5; M6, M7; M8, M9; M10, M11) simultaneously in test mode based on one memory block (M5; M7; M9; M11) which has a largest address space among said memory blocks (M4, M5; M6, M7; M8, M9; M10, M11); and
 - control means (16; 46; 56) for disabling writing in other memory blocks (M4; M6; M8; M10) having a smaller address space than said largest address space during an address scan period exceeding address widths of said other memory blocks (M4; M6; M8; M10).
2. A semiconductor integrated circuit comprising:
 - a writable/readable first memory block (M5) having a first address space;
 - at least one writable/readable second memory block (M4), mounted on a same chip as said first memory block (M5) and having an address space smaller than said first address space, said second memory block (M4) and said first memory block (M5) sharing part of an addresses in normal operation mode;
 - means for supplying address signals (A0 to A6) to simultaneously and commonly scan addresses of said first and second memory blocks (M5, M4) in test mode;
 - an address decoder (11, 12, 13) for selecting addresses of said first and second memory blocks based on said address scan signal; and
 - a control circuit (16) for disabling write/read operations on said second memory block (M4) in said test mode during a period in
- which said address signals exceed said address space of said second memory block (M4).
3. A semiconductor integrated circuit according to claim 2, characterized in that said control circuit (16) decides part of said address signals to detect a period in which said address signals exceeds said address space of said second memory block (M4) to thereby perform writing disable control.
4. A semiconductor integrated circuit according to claim 2, characterized by further comprising a logic circuit (38, 39), mounted on the same chip, for supplying said address signals.
5. A semiconductor integrated circuit according to claim 2, characterized in that said first and second memory blocks are a cache memory.
6. A semiconductor integrated circuit comprising:
 - a writable/readable first memory block (M9) having a first address space;
 - at least one writable/readable second memory block (M8), mounted on a same chip as said first memory block (M9) and having an address space smaller than said first address space, said second memory block (M8) and said first memory block (M9) not sharing part of addresses in normal operation mode;
 - a logic circuit (48), mounted on the same chip as said first memory block (M9), for supplying address signals to simultaneously and commonly scan addresses of said first and second memory blocks (M9, M8) in test mode;
 - an address selector (40) for selecting part of address signals to perform address scan of said first memory block (M9) and generating address signals of said second memory block (M8) in test mode;
 - an address decoder (42, 41) for selecting addresses of said first and second memory blocks (M9, M8) based on said address signals from said logic circuit (48) and said address selector (40); and
 - a control circuit (46) for disabling write/read operations on said second memory block (M8) in said test mode during a period in which said address signals of said first memory block (M9) exceeds said address space of said second memory block (M8).
7. A semiconductor integrated circuit according to claim 6, characterized in that said control circuit (46) decides part of said address signals to detect a period in which said address signals exceeds said address space of said sec-

ond memory block (M8) to thereby perform writing disable control.

8. A semiconductor integrated circuit comprising:
- a writable/readable first memory block (M1) having a first address space; 5
 - at least one writable/readable second memory block (M10), mounted on a same chip as said first memory block (M11) and having an address space smaller than said first address space, said second memory block (M10) and said first memory block (M11) not sharing part of addresses in normal operation mode; 10
 - a self-testing address generator (50), mounted on the same chip as said first memory block (M11), for supplying address signals to simultaneously and commonly scan addresses of said first and second memory blocks (M11, M10) in test mode; 15
 - an address selector (57, 58) for selecting said address signals to generate address signals of each of said memory blocks (M10, M11) in test mode; 20
 - an address decoder (51, 52) for selecting addresses of said first and second memory blocks (M11, M10) based on said address signals from said address selector (57, 58); and 25
 - a control circuit (56) for disabling write/read operations on said second memory block (M10) in said test mode during a period in which said address signals to commonly perform address scan of said memory blocks exceeds said address space of said second memory block (M10). 30
- 35
9. A semiconductor integrated circuit according to claim 8, characterized in that said control circuit (56) decides part of said address signals to detect a period in which said address signals exceeds said address space of said second memory block (M10) to thereby perform writing disable control. 40
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- 50
- 55

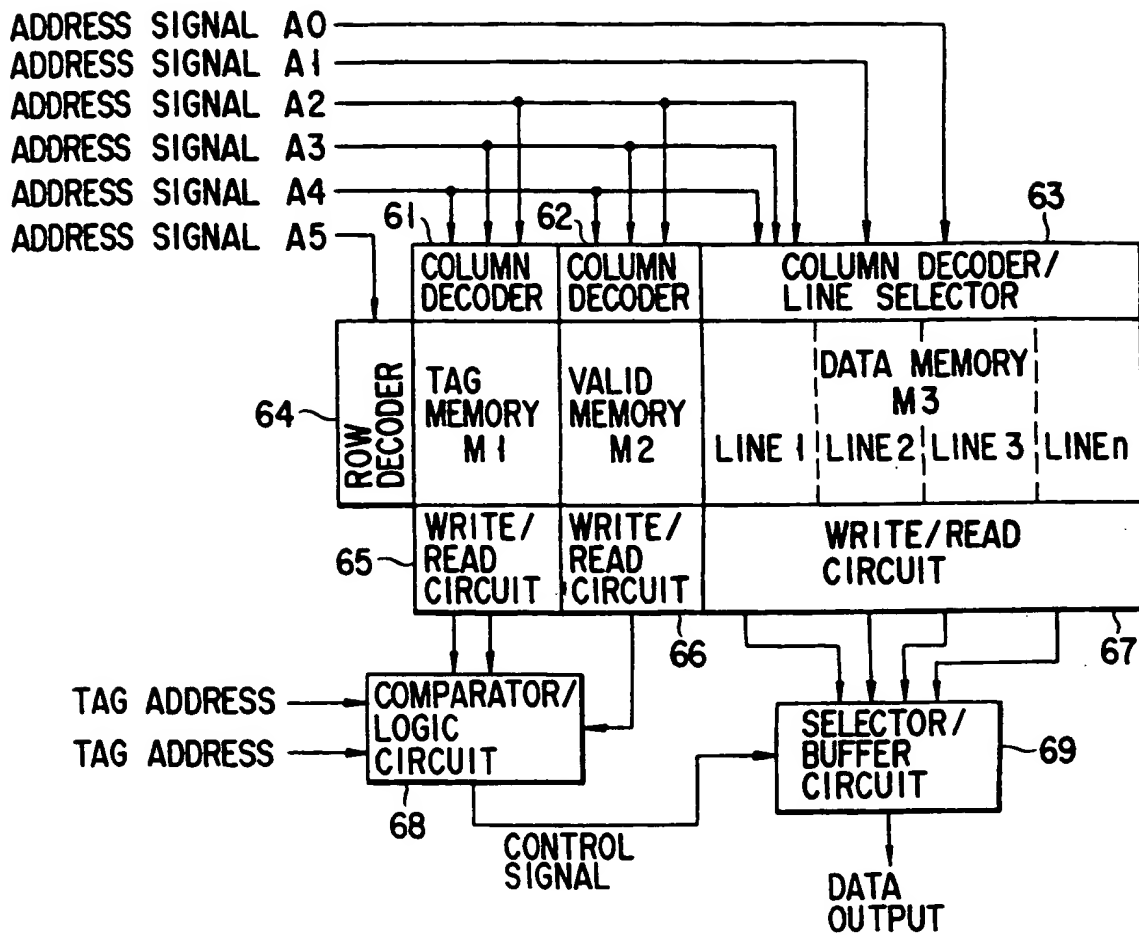
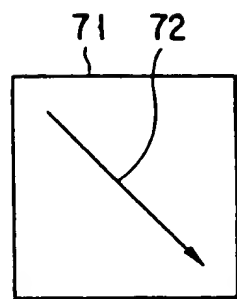


FIG. 1



WRITE ALL "0"

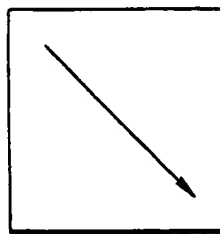
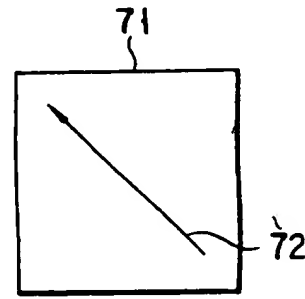
READ "0" AND
WRITE "1" IN
SAME CELLREAD "1" IN A
DIRECTION FROM A
LARGER ADDRESS
TO A SMALLER ONE
AND WRITE "0" IN
SAME CELL

FIG. 2A

FIG. 2B

FIG. 2C

A3 A2	A3 A2 A1 A0	
0 0	0 0 0 0	ACCESS TO CELL ①
0 0	0 0 0 1	ACCESS TO CELL ①
0 1	0 0 1 0	ACCESS TO CELL ①
1 0	0 0 1 1	ACCESS TO CELL ①
1 1	0 1 0 0	ACCESS TO CELL ②
1 1	0 1 0 1	ACCESS TO CELL ②
1 1	0 1 1 0	ACCESS TO CELL ②
1 1	0 1 1 1	ACCESS TO CELL ②

MEMORY BLOCKS
M1 AND M2
HAVING SMALL
ADDRESS SPARE

FIG. 3A-I

FIG. 3A-II

A3	A2	A1A0	A1A0	A1A0	A1A0
0	0	0	1	1	1
0	0	1	1	0	1
0	1	0	1	0	1
1	0	0	1	0	1
1	1	0	1	0	1

MEMORY BLOCKS M3
HAVING LARGER
ADDRESS SPARE BY
A₀ AND A₁

A3 A2 A1 A0

0	0	0	0	ACCESS TO CELL ①
0	0	0	1	ACCESS TO CELL ②
0	0	1	0	ACCESS TO CELL ③
0	0	1	1	ACCESS TO CELL ④
0	1	0	0	ACCESS TO CELL ⑤

FIG. 3B-I

FIG. 3B-II

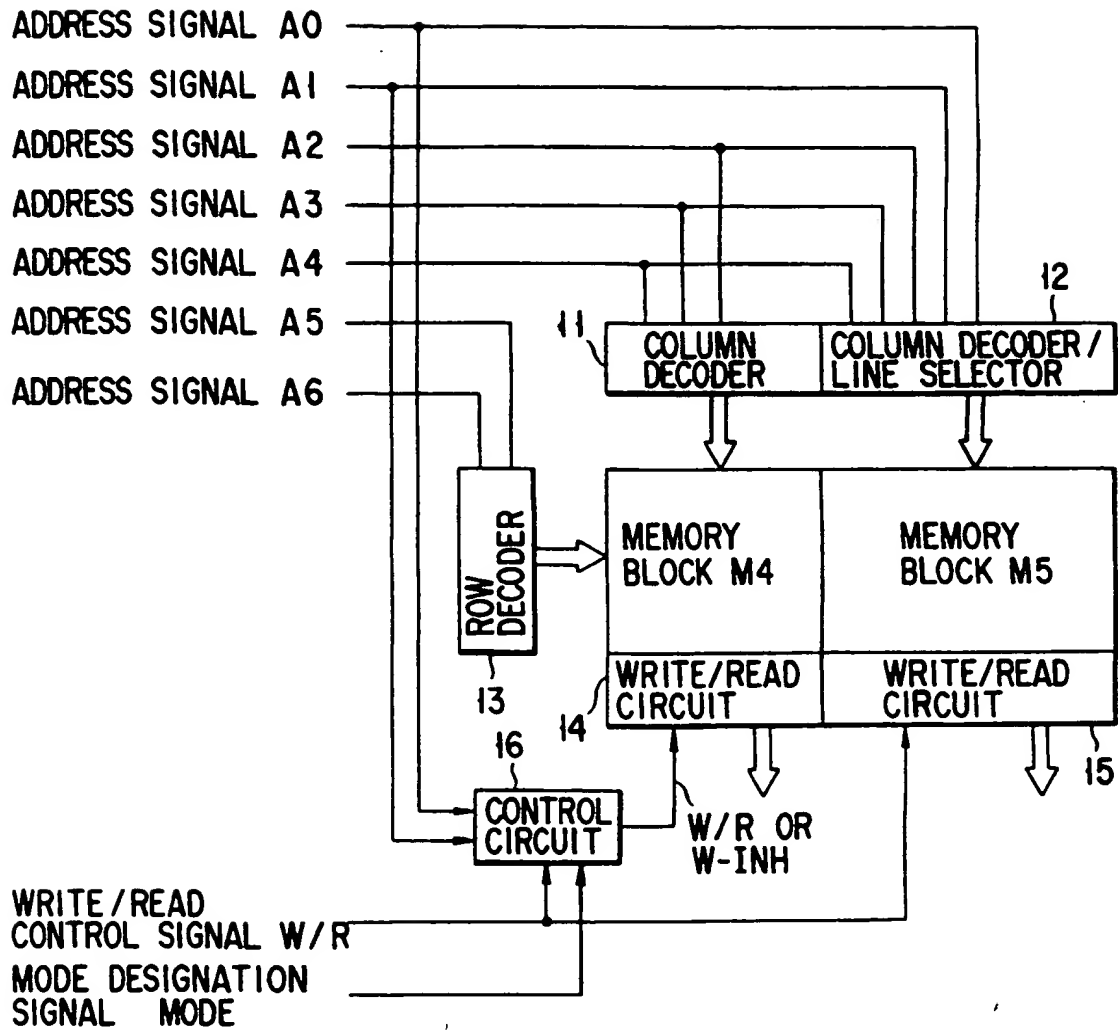


FIG. 4

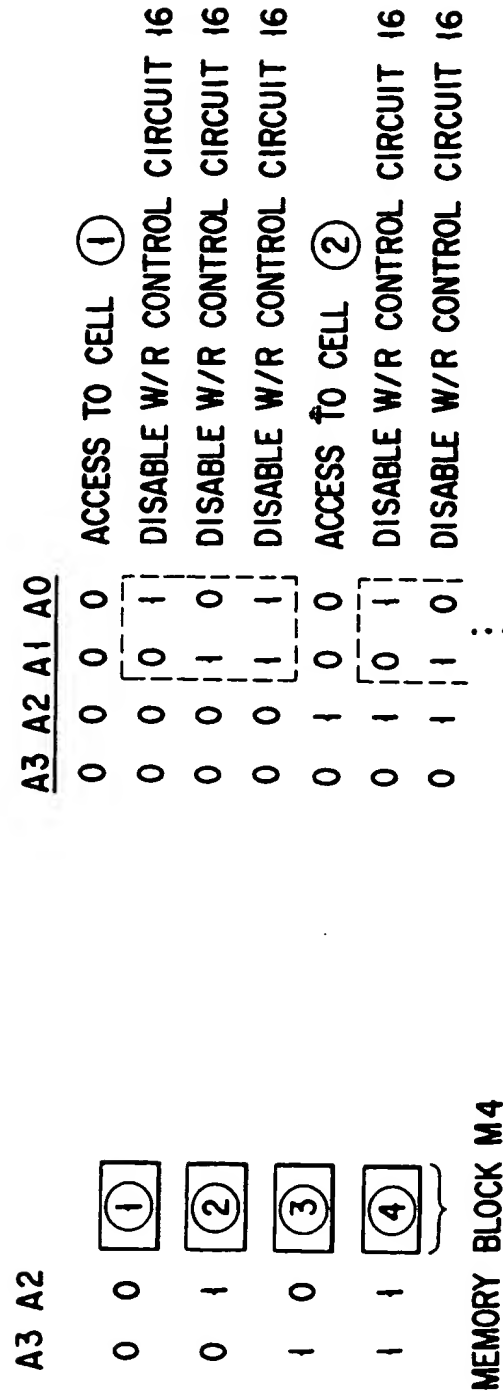


FIG. 5A-I

FIG. 5A-II

A3	A2	A1A0	A1A0	A1A0	A1A0
0	0	0	0	1	1
0	0	1	1	0	0
1	0	1	0	1	1
1	1	0	0	1	1
0	0	0	0	0	0
0	0	0	0	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0

A3 A2 A1 A0

ACCESS TO CELL ①
ACCESS TO CELL ②
ACCESS TO CELL ③
-ACCESS TO CELL ④
ACCESS TO CELL ⑤

MEMORY BLOCKS M5

FIG. 5B-I

FIG. 5B-II

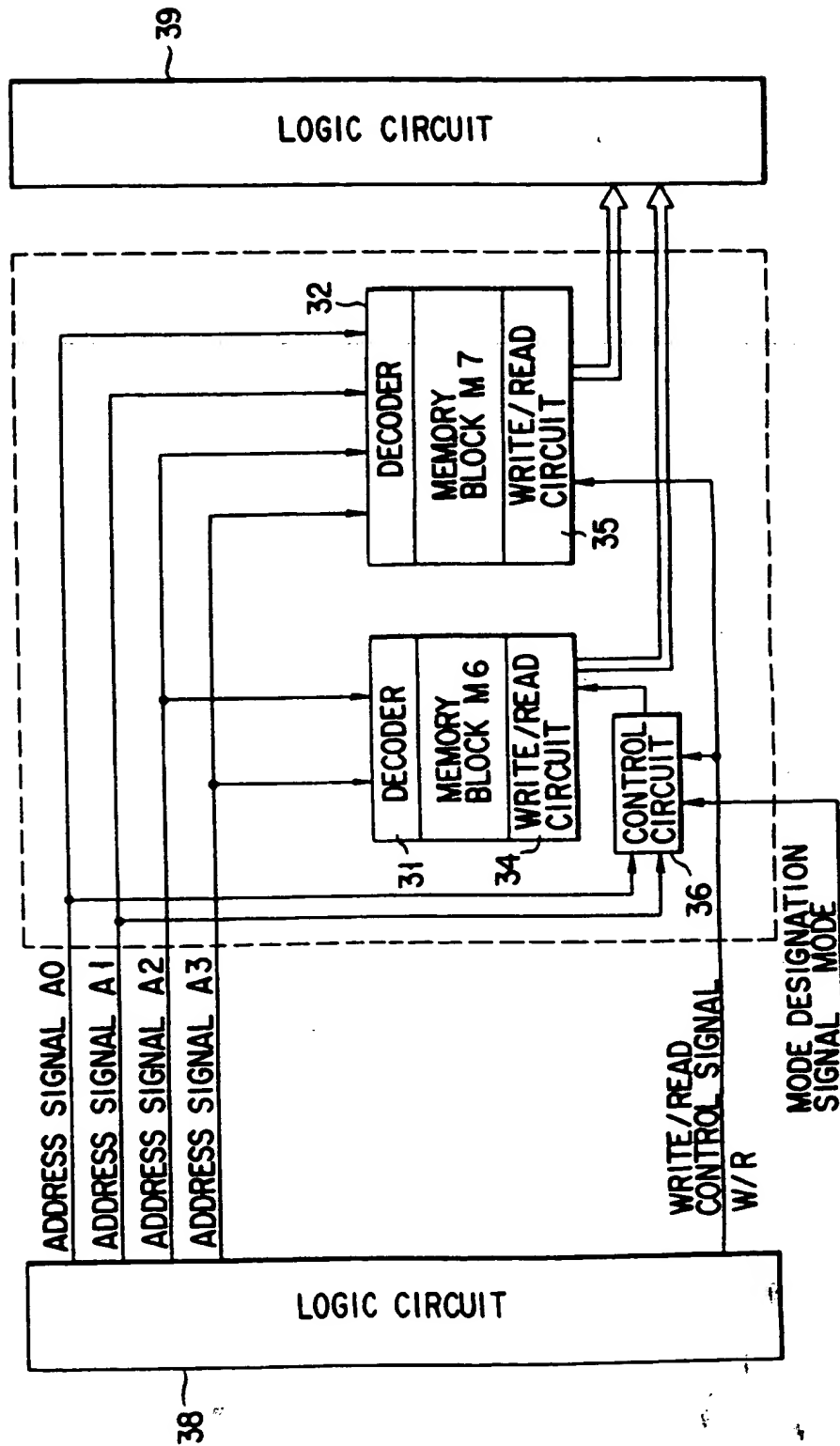


FIG. 6

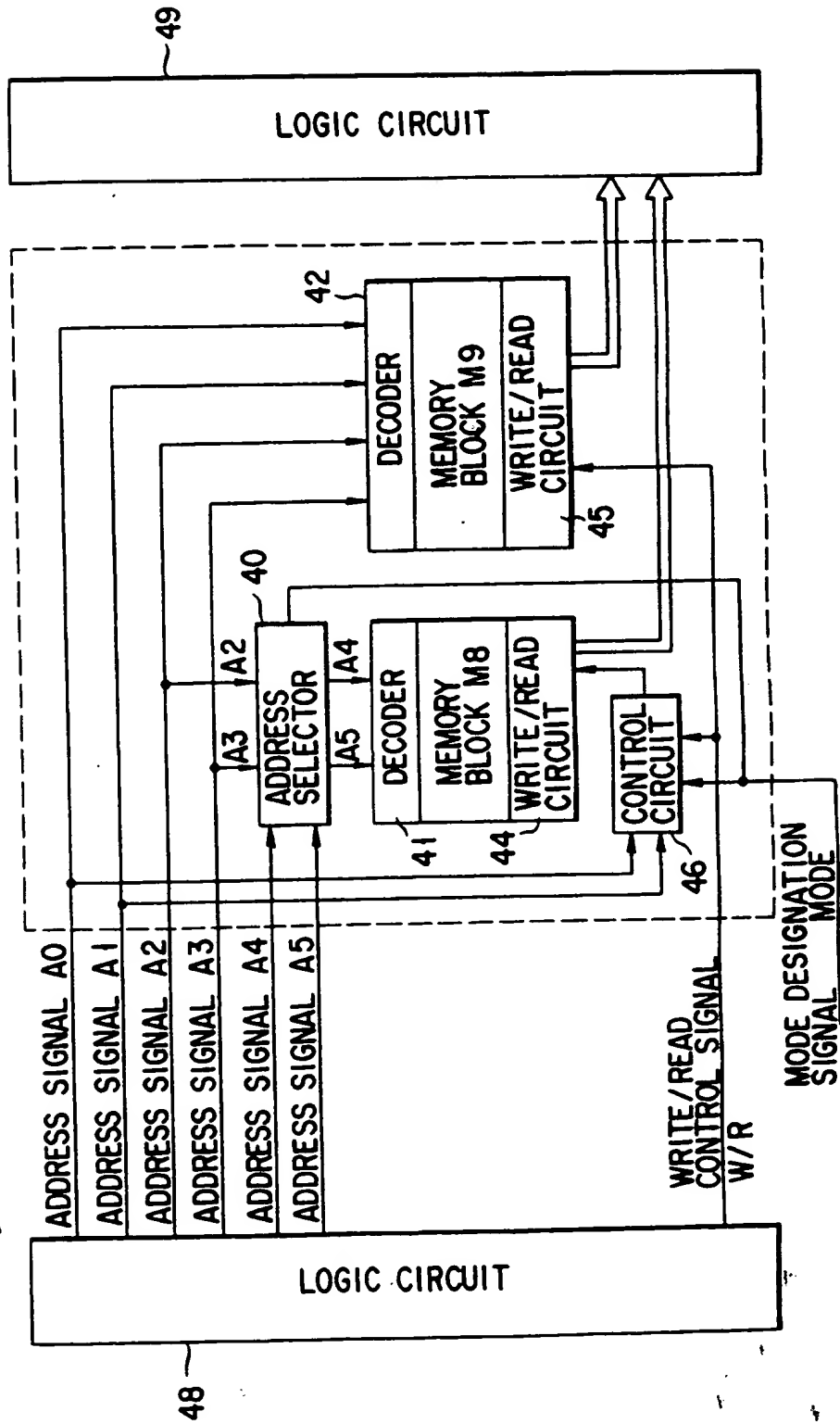


FIG. 7

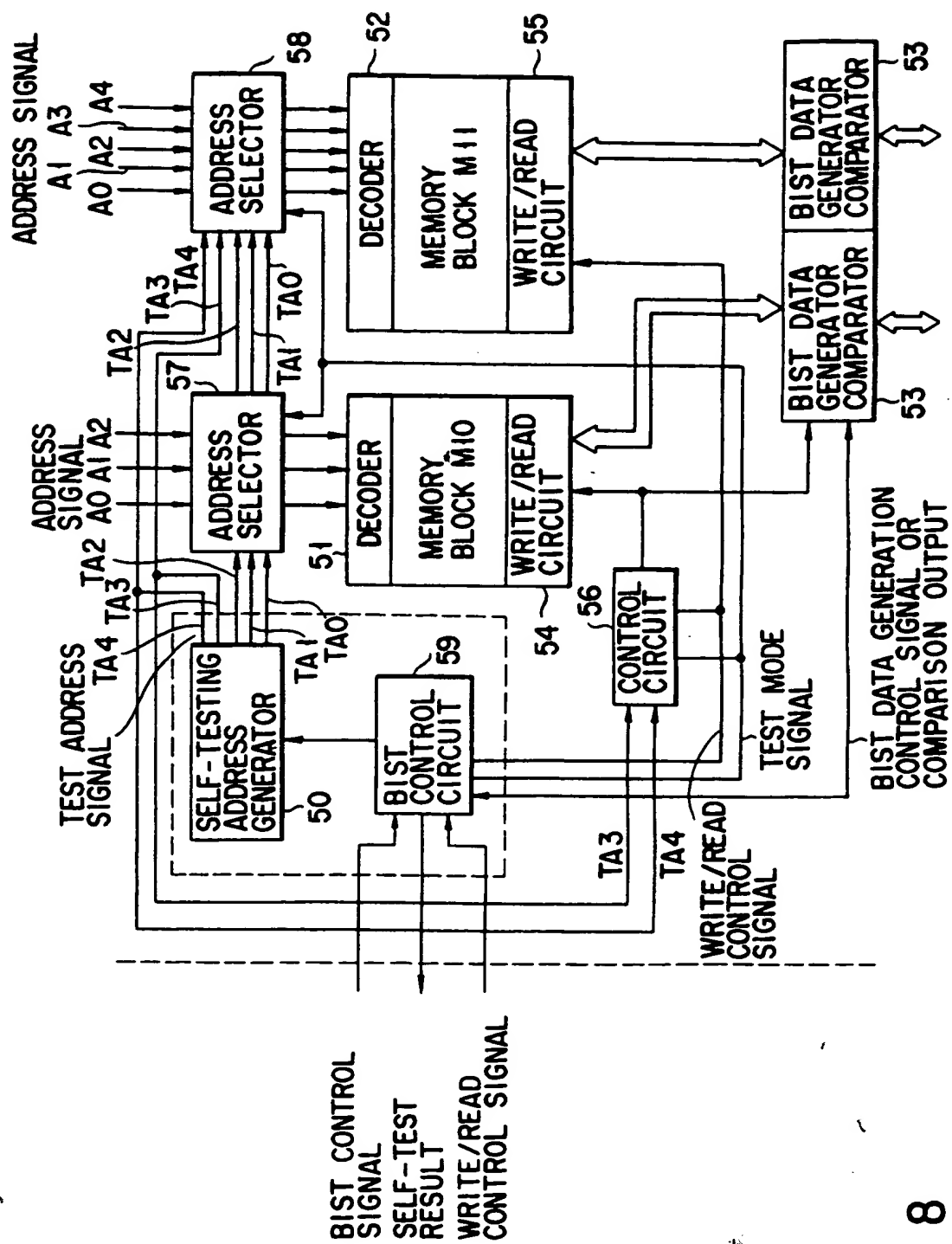


FIG. 8



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 12 2220

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 385 591 (NORTHERN TELECOM LTD) " column 9, line 43 - column 11, line 16 " " figures 6,7 "	1,2,6,8	611C29/00
A	--- 'INTERNATIONAL TEST CONFERENCE 1987 PROCEEDINGS, 1st - 3rd September 1987, Washington D.C., US, pages 826 - 833, IEEE, New York, US; L. BASTO et al.: 'Testing the MC68030 caches' " the whole document "	5	
A	--- NACHRICHTEN TECHNIK ELEKTRONIK, vol. 36, no. 9, 1986, BERLIN DD pages 333 - 335; W. FINSTERBUSCH: 'Speicherschaltkreis mit selbsttestenden Eigenschaften' " the whole document "	6,8	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G11C
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 07 APRIL 1992	Examiner MASCHE C.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : member of the same patent family, corresponding document			

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